an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;

side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;

a second silicon nitride film covering surfaces of said control gate, a source diffusion layer, a drain diffusion layer and each of said side walls of each of said memory transistors and on surfaces;

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a wiring layer formed over said second silicon nitride film via an inter-layer insulating film; and

element separating regions extending along one direction; and wherein

groups of said memory transistors are arranged along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate extending in said one direction;

each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions; and

said control gates extending in a direction perpendicular to said one direction and intersecting said memory transistors and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element separating regions.

Rewrite claim 17 as follows:

SUB E2 17. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate formed over said semiconductor substrate via a first gate insulating film and a control gate formed over said floating gate via a second gate insulating film;

an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;

side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;

a second silicon nitride film covering surfaces of said control gate, a source diffusion layer, a drain diffusion layer and each of said side walls of each of said memory transistors and on surfaces;

a wiring layer formed over said second silicon nitride film via an inter-layer insulating film; and

element separating regions extending along one direction, wherein

groups of said memory transistors are arranged along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate extending in said one direction;

each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions;

said control gates extending in a direction perpendicular to said one direction and intersecting said memory transistors and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element separating regions;

in each of said memory transistor, both said oxide film and another oxide film are formed between each said side wall and each said floating and control gates, and are formed between each said side wall and said substrate; and

in each said element separating region, both said oxide film and said another oxide film are formed between each said side wall and each said [floating and] control gates, and only said another oxide film is formed between each said side wall and each element separating insulating film.